Fabrication and Characterization of Pseudo-MOSFETs

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1 Introduction

In recent years, microelectronics has undergone an enormous evolution with a steadily increasing performance and complexity of integrated circuits that has been made possible by modern CMOS technology. Figure 1 shows a schematics of a conventional n-type bulk-Si MOSFET consisting of highly n-type doped source and drain areas within a p-type substrate. In addition, a MOSFET features a gate electrode of length $L$ and width $W$ that is insulated from the bulk-Si substrate by an insulator (typically SiO$_2$) of thickness $d_{\text{ox}}$. The two p-n-junctions at the source-channel and channel-drain interfaces (see Fig. 1 (b)) prevent a current from flowing from source to drain. Applying a positive gate voltage $V_{gs}$, an inversion layer is created at the channel/gate oxide interface since negative charge is injected into the channel from the source/drain contacts. If in addition a source-drain bias is applied, a current flows through the device.

The saturation current through a MOSFET is to first order given by the following expression:

$$I_d \approx \mu_{\text{eff}} \frac{W}{L} C_{\text{ox}} \frac{(V_{gs} - V_{\text{th}})^2}{2}$$

(1)

where $C_{\text{ox}} = \epsilon_{\text{ox}}/d_{\text{ox}}$ is the geometrical oxide capacitance per unit area, $\mu_{\text{eff}}$ is the effective carrier mobility and $V_{gs,\text{th}}$ are the gate and threshold voltages, respectively. Obviously, a higher current (which translates into a faster performing integrated circuit) is obtained when the channel length $L$ is scaled down and/or the effective carrier mobility is increased. In the past, a performance increase of MOSFET devices has almost exclusively been obtained by (down-)scaling the transistor dimensions. However, in the very near future continuing the down-scaling will become difficult due to a number of issues. One of the major obstacles is related to the appearance of so-called short channel effects (SCE), i.e. a loss of electrostatic gate control over the potential in the channel region. Short channel effects arise due to an overlap of the source-channel and channel-drain p-n-junctions yielding a strongly reduced potential barrier as illustrated in Fig. 1 (b). SCE are deleterious since they lead to drastically increased off-state leakage currents and thus to an enormous increase of the power consumption of highly integrated circuits. Therefore, some of the semiconductor industry’s main players have replaced the traditional bulk-Si substrates with silicon-on-insulator (SOI) technology.

SOI substrates consist of a thin silicon layer of thickness $d_{\text{SOI}}$ on top of a so-called buried oxide (BOX) of thickness $d_{\text{box}}$. A major benefit of SOI is that short channel effects can be suppressed effectively by scaling down the SOI-layer thickness $d_{\text{SOI}}$. Different types of SOI with ultrathin BOX and/or ultrathin top silicon layer, strained-silicon-on-insulator and even replacing the silicon completely with Germanium have been investigated intensively in recent years. In order to characterize the SOI-substrates a fast turn-around characterization method is required. To this end so-called Pseudo-MOSFETs are fabricated for the extraction of e.g.
the carrier mobility (explained in detail below). In the present lab-training, such Pseudo-MOSFET devices on SOI will be fabricated and characterized.

![Figure 1: (a) Schematics of a conventional bulk-Si MOSFET. (b) Illustration of the appearance of short channel effects in a scaled device: the white line represents the conduction band along current transport direction in a long-channel device. In a device suffering from SCE, the source-channel and channel-drain p-n-junctions overlap leading to a lowering of the potential barrier in the channel (green solid line). As a result, devices exhibiting SCE show an exponentially increased off-state leakage leading to a drastic increase of power consumption and eventually a loss of the ability to switch the device.]

2 The pseudo-MOSFET

In SOI substrates the active silicon layer is separated from a silicon handle wafer by a (rather thick) oxide, called the buried oxide (BOX). The idea of the pseudo-MOSFET is to use this buried oxide as the actual gate oxide and the silicon handle wafer as the gate electrode. In this case, only source and drain contacts have to be defined in order to realize a MOSFET structure. Hence, the pseudo-MOSFET concept allows a quick and straight-forward realization of MOSFETs and is therefore widely used to study SOI material.

In order to characterize the SOI material, in particular with respect to mobility, a simple model for the current through a MOSFET is employed: For small $V_{ds}$ the drain current $I_d$ increases linearly with drain voltage. In this so called linear regime of the output characteristics (i.e. $I_d$ versus drain-source voltage $V_{ds}$ for different gate voltages $V_{gs}$) the current is given by

$$I_d = f_g C_{ox} \frac{\mu}{1 + \theta(V_{gs} - V_{th})} \cdot (V_{gs} - V_{th})V_{ds}. \quad (2)$$

Again, $C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{d_{ox}}$ is the gate oxide capacitance per unit area and $d_{ox}$ is the buried oxide thickness in the present case. $V_{th}$ is the threshold voltage, i.e. the gate voltage where the device switches from the off- to the on-state and $f_g$ is a
factor that accounts for the geometry of the device. The factor $\theta$ takes series resistances into account, and is considered independent of the gate voltage.

Figure 2 (a) and (b) show the output and transfer characteristics of a MOSFET. An important figure of merit of a MOSFET in the on-state is the so-called transconductance $g_m$ which is the derivative of the drain current with respect to gate voltage:

\[
g_m = \frac{\partial I_d(V_{ds} = \text{const.})}{\partial V_{gs}}
\]  

Figure 2: Schematic cross section (a), output (b) and transfer (c) characteristics of a MOSFET.

The quality of the SOI material is reflected in the electronic transport properties of the material, i.e. in the effective carrier mobility $\mu$. In order to determine the mobility $\mu$ from the device characteristics we use the so-called $I_d/\sqrt{g_m}$-method since it provides values for $\mu$ which are not influenced by parasitic series resistances. With Eqn. (2) and (3) it is easy to show that

\[
\sqrt{f_g \mu C_{ox} V_{ds}(V_{gs} - V_{th})} = \frac{I_d}{\sqrt{g_m}}
\]  

Therefore, measuring $I_d$ versus $V_{gs}$ at small drain-source bias (typically 0.05 to 0.1V), calculating $g_m$ and plotting $I_d/\sqrt{g_m}$ versus $V_{gs}$ yields a straight line. The slope of this line is simply $\sqrt{f_g \mu C_{ox} V_{ds}}$ from which the mobility $\mu$ can be extracted provided that the geometry factor $f_g$ is known. In rectangular MOSFETs $f_g$ is the ratio of channel width and channel length $f_g = W/L$. However, since in our experiment we deal with circular pseudo-MOSFETs the geometry factor is a little more complicated. Nevertheless, a closed expression for the ratio between width and length can be computed also in the circular case: $f_g = \frac{2r}{\ln(R/r)}$ where $R, r$ are radii of the circular pseudo-MOSFET as shown in Fig. 5.
### 3 Device Fabrication

The fabrication of the devices will be carried out in the clean room facility of the Institute of Semiconductor Electronics. The advisor will instruct the participants how to dress and how to behave in the clean room. In order to avoid contamination participants have to wear gloves at all times when being in the clean room. Protective clothing such as apron, a second pair of gloves with sleeves and a face shield is mandatory when working with hazardous chemicals.

Each participant will get one SOI sample for the pseudo-MOSFETs. In addition, a bulk silicon substrate will be cleaved and every participant will get as many dummy samples as needed. The fabrication procedure is listed below. During your lab-work, protocol the fabrication process and take as many notes as necessary since this will be attached to the written report as an appendix.

**Mesa definition:**

- a bulk silicon wafer (dummy samples) is coated with TI Prime (30sec @ 3000rpm, 2min @ 120°C) and photoresist (AZ 5214, 30sec @ 3000rpm, 90sec @ 95°C), and subsequently cleaved into $2 \times 2$ cm$^2$ pieces with a diamond scribe.

- remove the photoresist with acetone, rinse in propanol, blow dry

- dehydration of the samples on a hot plate at 120°C for 5 minutes

- apply TI Prime (see above) to the dummy samples and the SOI sample

- spin-on photo resist (AZ 5214) at 3000rpm; pre-bake on a hot plate 95°C for 90sec

- 1st lithography with mask-aligner: expose the sample with 15mW/cm$^2$ for 7s

- develop for $\sim$30s (AZ 726 MIF), rinse thoroughly in DI water, blow dry

- post-exposure bake on hot plate at 110° for 5 minutes

- for mesa etching mix 50ml H$_2$O, 100ml HNO$_3$ and 5ml BOE (buffered oxide etch). Note the order of the chemicals!! Caution: BOE contains hydrofluoric acid (HF), an extremely hazardous chemical that can lead to severe injuries.

- determine the etch rate of the chemical solution by etching dummy samples for several different durations, remove the resist in acetone, rinse in propanol, blow dry with nitrogen and measure the etch depth with a surface profiler/confocal laser microscope
• determine the expected etch duration, etch the SOI sample until you see that the SOI is fully etched through and rinse immediately afterwards in DI water

• remove the photoresist in acetone, rinse in propanol, blow dry

Figure 3: Schematics of the mesa etch process.

**Contact formation**

• dehydration of sample on a hot plate at 120°C for 5 minutes

• apply TI Prime (see above)

• resist (AZ 5214) spin-on at 3000rpm; pre-bake on a hot plate at 95°C for 90s

• 2nd lithography, image reversal process. Expose the samples for 2s followed by a post-exposure bake on the hot plate at 115°C for 2min; flood exposure for 9sec

• develop in AZ 726 MIF for ~35s, rinse thoroughly in DI water, blow dry

• dip in BOE solution for 10s, rinse in DI water for 2 minutes, blow dry; the samples are then mounted immediately in an e-beam evaporation chamber and aluminum (100nm) is deposited.

• after deposition, put the samples in acetone, lift-off aluminum, rinse in propanol and blow dry with nitrogen

Figure 5 shows a scanning electron microscopy image of a readily fabricated circular pseudo-MOSFET. The width and channel length of the device are shown as well. The buried oxide (BOX) serves as the actual gate oxide as already mentioned above.
4 Electrical Measurement and Characterization

Electrical measurements will be performed with Semiconductor Parameter Analyser. The sample will be mounted in a probe station as schematically shown in Fig. 6. The following measurements and characterizations should be made:

- Measure (all devices) the drain current versus gate voltage (transfer characteristics) over a large gate voltage range (e.g. ±40V) for drain voltages of up to 2V starting at 0.1V. Plot the transfer characteristics on a linear and a log-scale plot. Compare the on-currents, the leakage currents due to the ambipolar behavior and the inverse subthreshold slopes of the different devices.

- Measure (all devices) the output characteristics over the same drain and gate voltage range. Plot the output characteristics.

- Extract the mobility of the fabricated samples using the $I_d/\sqrt{g_m}$-method. Plot the mobility versus the channel length of the different devices.
5 Writing your Report

After the characterization you are supposed to write a short report. Since writing reports is often considered as being boring you should write it with the following background:

After finishing your MSc degree at RWTH Aachen University you work for an up-and-coming consulting company in the semiconductor industry. Your speciality is the implementation of new materials into existing CMOS production lines and you have been called by the CTO (chief technical officer) - one of your friends - of a foundry that has been producing logic ICs with conventional bulk silicon substrates. The CEO (chief executive officer) of the foundry has only a limited technical background but has to decide between several technology options. To save costs he would like to run the standard bulk silicon process also when producing the next generation CMOS circuits. Furthermore, he suspects that the carrier mobility in SOI is lower compared to bulk and that moving to SOI does not pay off.

The CTO on the other hand calculated that the next generation devices would suffer from SCE so severe that they cannot be used for the company’s products anymore. He argues that the company has to move from bulk to SOI substrates which, however, implies a severe financial investment into new fabrication tools.

The CTO discusses her findings with the CEO who is absolutely not amused and tells your friend that he recently read in the PM! magazine that the mobility in SOI is worse than in bulk and moving to SOI technology would not pay-off since the financial investments would be too cost-intensive. Your friend agrees but replies that the investments are necessary in order to keep-up with the company’s competitors and that SOI is the way to go. The CTO is worried that the CEO will ruin the company with launching a new product that will eventually exhibit
a worse performance than its predecessors. So, she decides to hire you to perform a technical study on SOI MOSFETs. You should convince the CEO to go for SOI technology in the following way:

- Write a cover letter stating your recommendation, the key benefits of using SOI technology. Point out to the enclosed material that backs up your recommendation (the technical annex which contains the results of your experimental work). Remember that the CEO has only a limited technical background - he understands dollars not MOSFETs. Therefore, the style of the letter should be a mixture of business- and technical-like. But most of all it should be convincing! You might want to use this opportunity to give your consulting company a fancy name.

- Prepare a technical annex. In this annex you should explain and discuss the pseudo-MOSFET results. You should also state and explain shortly the method you used to obtain the mobility data and the experimental procedure. To this annex your lab notes should be added. Refer to these notes in the technical annex.

The report can either be written in German or English.

**Bibliography**

