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Fabrication and Characterization of Ψ-MOSFETs

as experiment M8 within the lab course

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1 Introduction

In recent years, microelectronics has undergone an enormous evolution with a steadily increasing performance and complexity of integrated circuits that has been made possible by modern CMOS technology. Figure 1(a) shows a schematic of a conventional n-type bulk-Si MOSFET consisting of heavily n-type doped source and drain areas within a p-type substrate. In addition, a MOSFET features a gate electrode of length L and width W that is insulated from the bulk-Si substrate by an insulator (typically SiO_2) of thickness d_{ox}. The two p-n-junctions at the source-channel and channel-drain interfaces (see Figure 1(b)) prevent a current from flowing from source to drain. Applying a positive gate voltage $V_{gs} > V_{th}$, an inversion layer (electrons in a p-type substrate) is created at the channel/gate oxide interface. In this case if an additional drain-source bias V_{ds} is applied, a current can flow through the device.

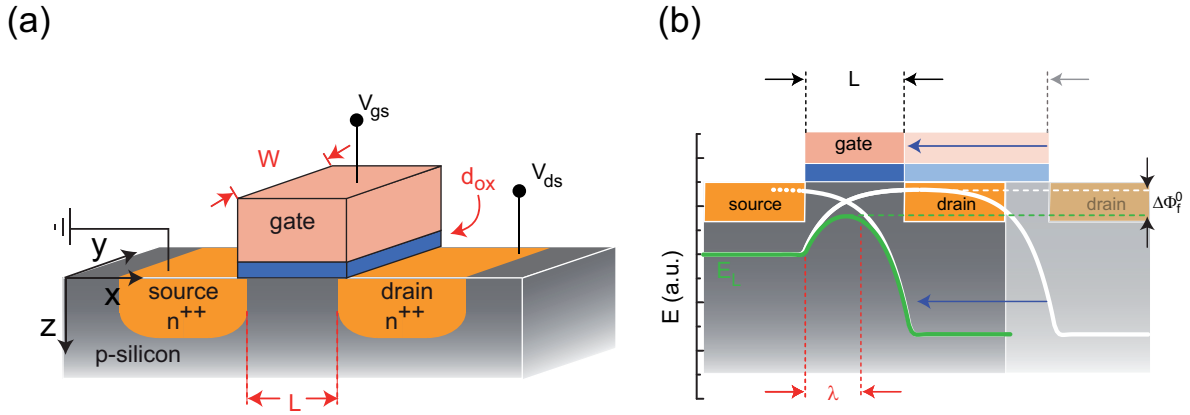


Figure 1: (a) Schematics of a conventional bulk-Si MOSFET. (b) Illustration of the appearance of short channel effects in a scaled device: the white line represents the conduction band along current transport direction in a long-channel device. In a device suffering from SCE, the source-channel and channel-drain p-n junctions overlap leading to a lowering of the potential barrier in the channel (green solid line). As a result, devices exhibiting SCE show an exponentially increased off-state leakage leading to a drastic increase of power consumption and eventually a loss of the ability to switch the device.

The saturation current through a MOSFET is to first order given by the following expression:

$$I_d \approx \mu_{eff} \frac{W}{L} C_{ox}^{\square} \frac{(V_{gs} - V_{th})^2}{2}, \qquad \text{with } V_{ds} > V_{gs} - V_{th} > 0 \tag{1}$$

where $C_{ox}^{\square} = \varepsilon_0 \varepsilon_{ox} / d_{ox}$ is the geometrical oxide capacitance per unit area, μ_{eff} is the effective carrier mobility and V_{gs}, V_{th} are the gate and threshold voltages, respectively. Obviously, a higher current (which translates into a faster performing integrated circuit) is obtained when the channel length L is scaled down and/or the effective carrier mobility μ_{eff} is increased. In the past, a performance increase of MOSFET devices has almost

exclusively been obtained by (down-) scaling the transistor dimensions. However, in the very near future continuing the down-scaling will become difficult due to a number of issues.

1.1 Short Channel Effects

One of the major obstacles is related to the appearance of so-called short channel effects (SCE), i.e. a loss of electrostatic gate control over the potential in the channel region. Short channel effects arise due to an overlap of the source-channel and channel-drain p-n-junctions, which yields a strongly reduced potential barrier as illustrated in Figure 1(b). SCE are deleterious since they lead to drastically increased off-state leakage currents and thus to an enormous increase of the power consumption of highly integrated circuits. Therefore, some of the semiconductor industry's main players have replaced traditional bulk-Si substrates with silicon-on-insulator (SOI) technology. SOI substrates consist of a thin silicon layer of thickness d_{SOI} on top of a so-called buried oxide (BOX) of thickness d_{BOX} like shown in Figure. 2.

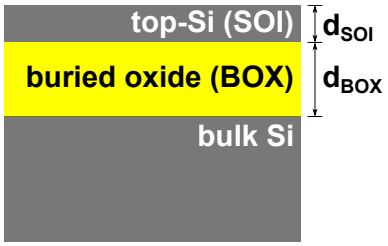
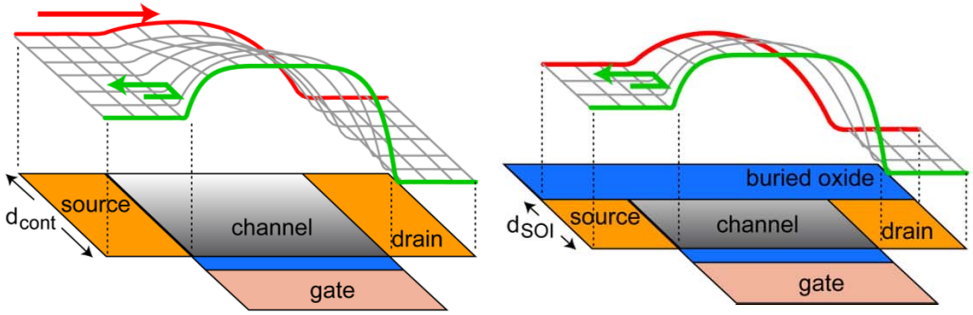


Figure 2: Schematic of an SOI wafer.



(a) (b)

Figure 3: Three-dimensional conduction band profiles for MOSFET devices based on (a) bulk-silicon and (b) silicon-on-insulator substrates.

A major benefit of SOI over bulk silicon is that short channel effects can be suppressed effectively by avoiding the leakage currents that flow at the bottom interface (red arrow in Figure 3 (a)), where the band profile is worse controlled by the gate than that near the gate oxide. Short channel effects can be further suppressed by scaling down the

SOI-layer thickness d_{SOI} upon which a MOSFET with a fully depleted channel can be realized. What's more, strained-silicon-on-insulator (SSOI) has recently been introduced as a "new" silicon material with up to 100 % increased mobility that allows combining scalability and performance improvements. As a result, SOI material is regarded as a promising alternative to achieve even higher circuit performance in the post Moore era.

1.2 Aim of the Lab Course

In order to characterize the SOI substrates a fast turn-around characterization method is required. To this end so-called Ψ-MOSFETs are fabricated for the extraction of e.g. the carrier mobility (explained in detail below). In the present lab-training, such Ψ-MOSFET devices on SOI will be fabricated and characterized. Concerning their electrical characteristics, Ψ-MOSFETs are low performance devices and as such they would never be used in practical applications, however they can be used to extract the relevant parameters of their substrate material. Despite the simplicity of their build-up, a variety of parameters could be extracted. Out of those, only the threshold voltage and the inverse subthreshold slope of the fabricated Ψ-MOSFET and the carrier mobility of the top silicon layer of the SOI material (see Figure 2) shall be determined within the scope of this lab course.

2 The Ψ-MOSFET

In SOI substrates the active top silicon layer is separated from a silicon handle wafer through a (rather thick) layer of oxide, called the buried oxide (BOX). The idea of the Ψ-MOSFET is to take advantage of the configuration of SOI material where the buried oxide is used as the actual gate oxide and the silicon handle wafer as the gate electrode. In this case, only source and drain contacts have to be defined on the top silicon layer in order to fabricate a MOSFET structure.

In order to characterize the SOI material, in particular with respect to mobility, a simple model for the current through a MOSFET is employed: For small V_{ds} the drain current I_{d} increases linearly with drain voltage. In this so called linear regime of the output characteristics (i.e. I_{d} versus drain-source voltage V_{ds} for different gate voltages V_{gs}) the current is given by

$$I_{\mathrm{d}} = f_{\mathrm{g}} C_{\mathrm{ox}}^{\square} \frac{\mu_{\mathrm{eff}}}{1 + \theta\,(V_{\mathrm{gs}} - V_{\mathrm{th}})} (V_{\mathrm{gs}} - V_{\mathrm{th}})\, V_{\mathrm{ds}}, \qquad \text{with } V_{\mathrm{gs}} - V_{\mathrm{th}} > V_{\mathrm{ds}} > 0 \tag{2}$$

Again, $C_{\mathrm{ox}}^{\square} = \varepsilon_0 \varepsilon_{\mathrm{ox}} / d_{\mathrm{ox}}$ is the gate oxide capacitance per unit area and d_{ox} is the buried oxide thickness in the present case. V_{th} is the threshold voltage, i.e. the gate voltage where the device switches from the off- to the on-state and f_{g} is a factor that accounts for the geometry of the device. The factor θ is the mobility attenuation factor that takes series resistances into account, and is considered independent of the gate voltage.

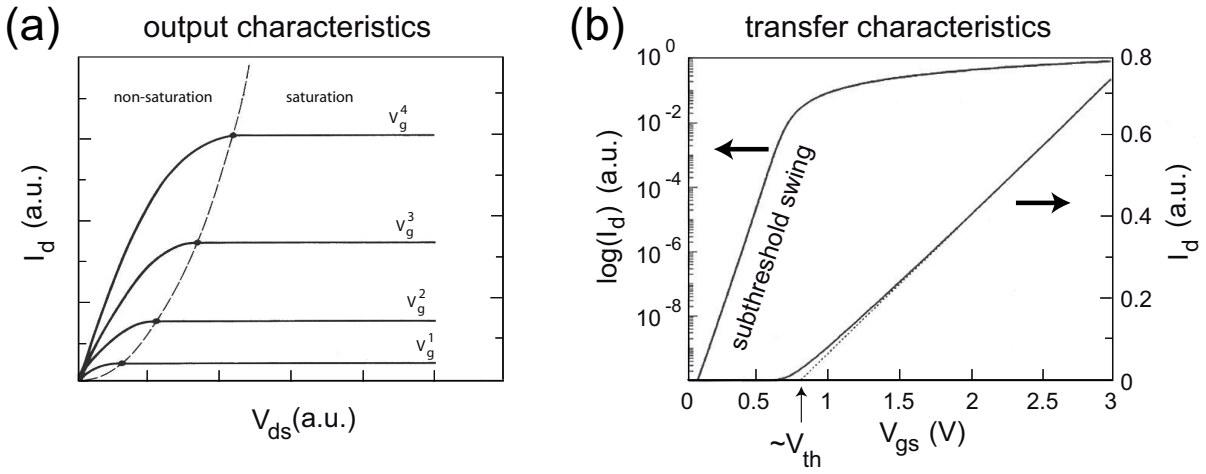


Figure 4: Output (a) and transfer (b) characteristics of a MOSFET.

Figure 4(a) and (b) show the output and transfer characteristics of a MOSFET. An important figure of merit of a MOSFET is the so-called transconductance g_{m} which is the derivative of the drain current with respect to gate voltage:

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}\,(V_{\mathrm{ds}} = \text{const.})}{\partial V_{\mathrm{gs}}} \tag{3}$$

The quality of the SOI material is reflected in the electronic transport properties of the material, i.e. in the effective carrier mobility μ_{eff}. In order to determine the mobility μ_{eff} from the device characteristics we use the so-called $I_{\text{d}}/\sqrt{g_{\text{m}}}$-method since it provides values for μ_{eff} which are not influenced by parasitic series resistances. With Eqn. (2) and (3) it is easy to show that

$$\sqrt{f_{\text{g}}\mu_{\text{eff}}C_{\text{ox}}^{\square}V_{\text{ds}}}\,(V_{\text{gs}}-V_{\text{th}}) = \frac{I_{\text{d}}}{\sqrt{g_{\text{m}}}} \tag{4}$$

Therefore, measuring I_{d} versus V_{gs} at small drain-source bias, calculating g_{m} and plotting $I_{\text{d}}/\sqrt{g_{\text{m}}}$ versus V_{gs} yields a straight line. The slope of this line is simply $\sqrt{f_{\text{g}}\mu_{\text{eff}}C_{\text{ox}}^{\square}V_{\text{ds}}}$ from which the mobility μ_{eff} can be extracted provided that the geometry factor f_{g} is known. In rectangular MOSFETs f_{g} is the ratio of channel width and channel length $f_{\text{g}} = W/L$. However, since in our experiment we deal with circular Ψ-MOSFETs the geometry factor is a little more complicated. Nevertheless, a closed expression for the ratio between width and length can be computed also in the circular case: $f_{\text{g}} = \dfrac{2\pi}{\ln(R_2/R_1)}$ where R_1, R_2 are radii of the circular Ψ-MOSFET as shown in Figure 10.

2.1 Principle of Operation

One might ask, why the Ψ-MOSFET is able to operate despite the simplicity of its build-up. In a conventional MOSFET the doping of source and drain areas leads to the formation of a barrier which can be manipulated by varying the gate voltage.

Figure 5 shows how the barrier is formed. The figure on the left shows the schematic band diagrams of all areas involved and still "separated", the right hand side is the result after their "connection". Please be aware that the term "connecting" is only an aid to understand the principle and doesn't describe the physical process. In the actual device a Fermi level equilibrium is established, causing the conduction and valence band edges in the channel to "elevate" and thus forming a *barrier* for electrons in source and drain areas. The height of the barrier is controlled by the electrostatic potential in the channel, which itself is being varied by the gate voltage applied.

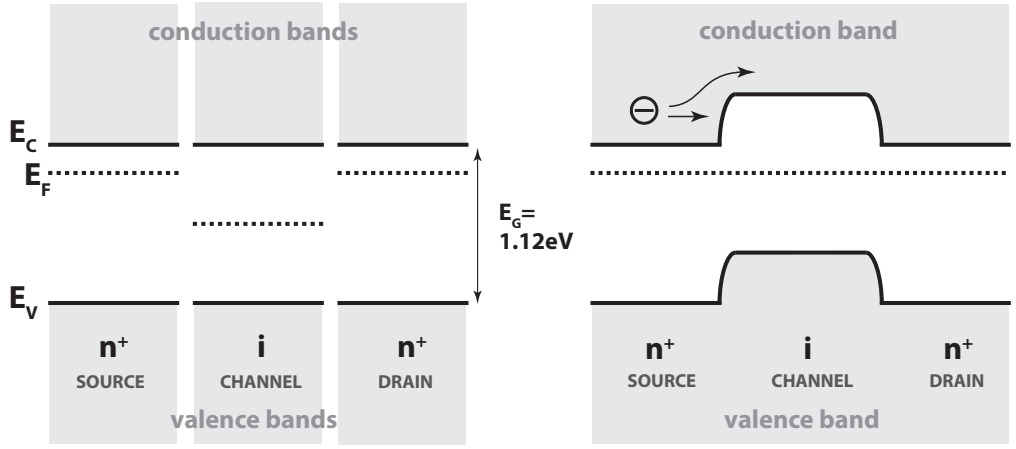


Figure 5: Schematic band diagrams of a conventional n-type MOSFET in silicon, in the case of separated (left figure) and continuous (right figure) areas in the device. E_V and E_C denote the band edges of valence and conduction band, respectively, E_F is the Fermi energy. In case of an average n-type doping ($= n^+$), $E_\mathrm{C} - E_\mathrm{F}$ is approx. 40...60 meV, 'i' denotes undoped (= intrinsic) areas. Here, the Fermi level is in the middle of the bandgap.

However, in a Ψ-MOSFET only the channel might (but doesn't even need to) be doped, whereas "source" and "drain" are plain metal contacts directly deposited on silicon. In order to exhibit a behaviour similar to a conventional MOSFET, another effect must be responsible for the voltage controllable current in the device. This effect is the formation of a *Schottky barrier*, which can be created upon the direct connection of a metal (i.e. Al) to a semiconductor. For a better understanding of this effect schematic band diagrams are of great importance.

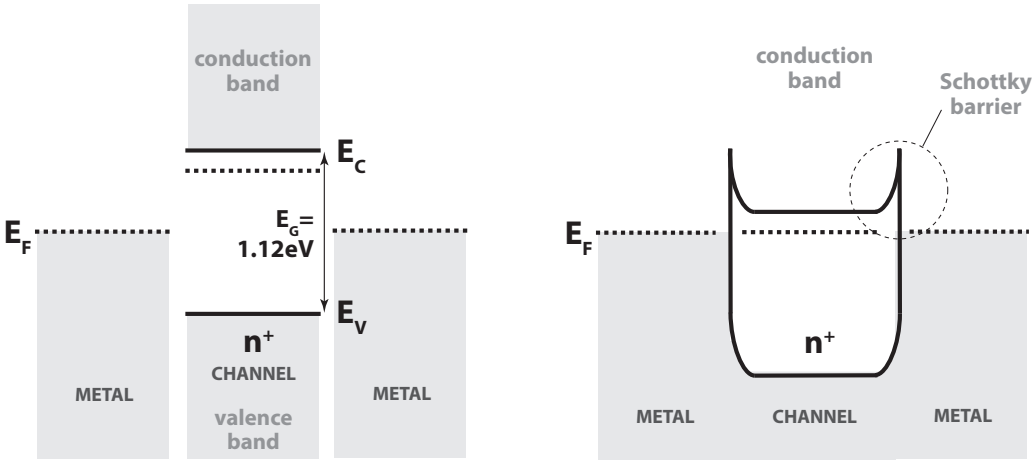


Figure 6: Schematic band diagram of a Ψ-MOSFET with n-channel in silicon (work function of metal larger than that of semiconductor: $\phi_\mathrm{m} > \phi_\mathrm{s}$), in the case of separated (left figure) and continuous (right figure) areas in the device. E_V and E_C denote the band edges of valence and conductance band, respectively, other indices as before.

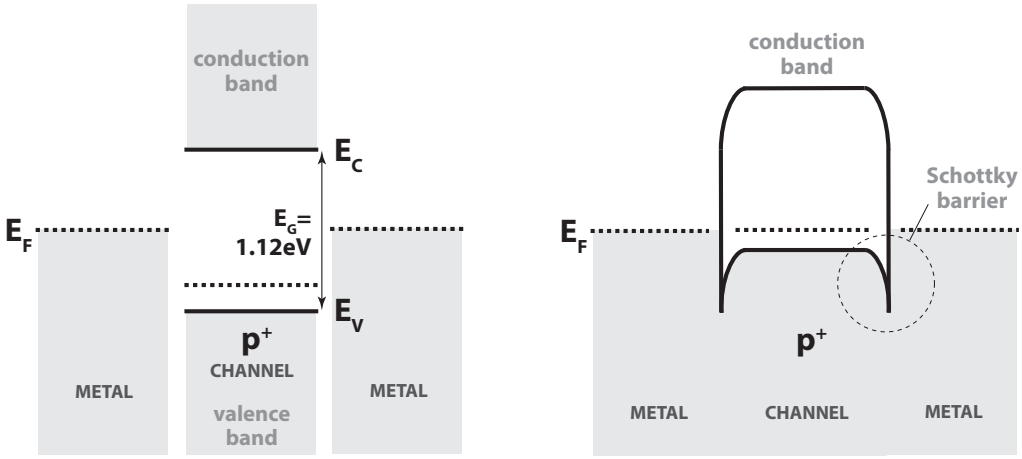


Figure 7: Schematic band diagram of a Ψ-MOSFET with p-channel in silicon (work function of metal smaller than that of semiconductor: $\phi_\mathrm{m} < \phi_\mathrm{s}$), in the case of separated (left figure) and continuous (right figure) areas in the device. E_V and E_C denote the band edges of valence and conductance band, respectively, other indices as before.

As soon as the semiconductor is brought into contact with a metal (aluminum in the case of this lab course), the Fermi level of the semiconductor and the Fermi level of the metal again establish a thermodynamic equilibrium. The occuring band deformation in consequence leads to the formation of a barrier. Note though, that the actual Schottky barrier is formed directly at the interface between metal and semiconductor. Thus, the "spikes" in Figure 6 and 7 at the transition between metal and channel are the actual Schottky barriers. The height of the Schottky barriers is determined by material parameters[1] and can't be influenced by the applied "gate" voltage. However, the electrostatic potential within the channel can be changed via the gate voltage and in consequence modify the height of the conductance and valance band edge in the channel. In case of a Ψ-MOSFET with p-channel in silicon like shown in Figure 8, the valence band will be pushed up with an increasing negative voltage so that the Schottky barrier width at the source-channel and drain-channel contacts will be thinner and becomes more transparent for holes. With an additional positive drain (or negative drain) voltage, holes can tunnel through the thin drain-channel (or source-channel) Schottky barrier to form a current flow through the device.

[1]Namely the work function ϕ_m of the metal and electron affinity χ of the semiconductor. In the case of an Al - Si contact the smallest possible barrier height is $E_\mathrm{B} = E_\mathrm{g} - e\,(\phi_\mathrm{m} - \chi) = 1.12\,\mathrm{eV} - (4.26\,\mathrm{eV} - 4.05\,\mathrm{eV}) = 0.91\,\mathrm{eV}$. This value is purely theoretical, as the actual barrier height is strongly influenced by surface contamination, surface defects, interface layers and imperfections. All these effects will, in practice, lead to a significantly increased barrier height.

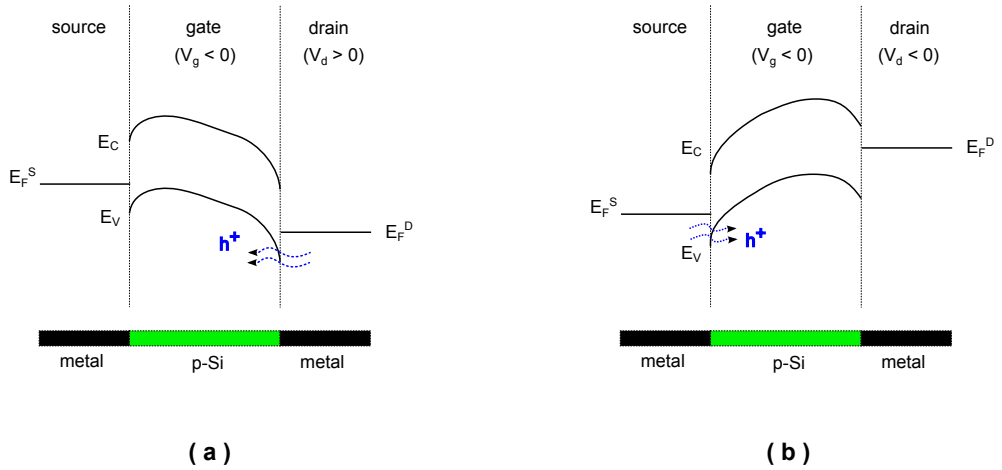


Figure 8: A Ψ-MOSFET with p-channel in silicon biased with negative gate voltage, the valence band will be pushed up so that the Schottky barrier width at the source-channel and drain-channel contacts becomes thinner. An additional positive drain voltage further narrows the drain-channel junction and injects holes from drain into the channel (a) and an additional negative drain voltage further narrows the source-channel junction and pulls holes from source into the channel (b).

Another feature of the Ψ-MOSFET is its ambipolarity like shown in Figure 9, which means that it can operate with positive and negative gate voltages and shows classical MOSFET characteristics for both regimes. For the measurement evaluation one has to make sure to use the right configuration of gate voltage and source-drain voltage: the majority carriers are different for different polarities! It can be holes or electrons to be the majority charge carriers contributing to the on-current, therefore the extracted parameters for carrier mobility and transconductance will be those for the respective carrier type.

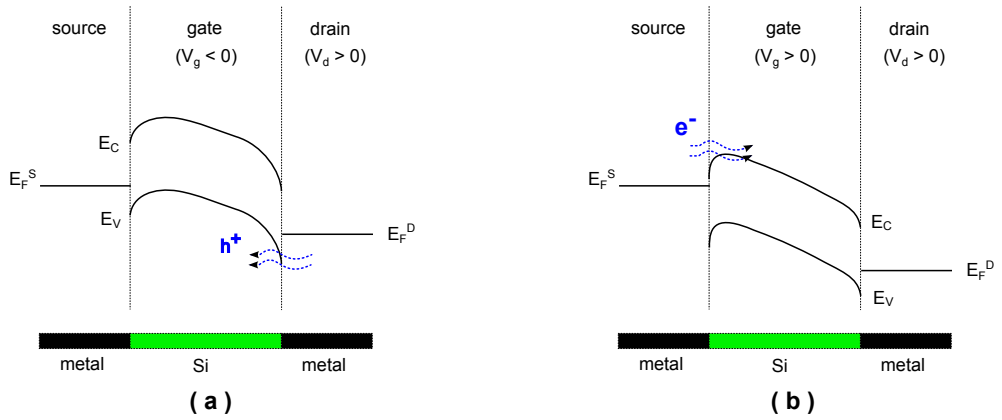


Figure 9: A Ψ-MOSFET with p-type silicon. If the gate is biased with negative voltage, the channel stays as a p-type channel, holes are injected from drain to channel with a positive drain voltage applied to the drain electrode (a) and if the gate is biased with sufficient positive voltage, the channel is then inverted into an n-type channel, thermally excited electrons can then pass the source-channel juction with an additional positive voltage applied to the drain electrode (b).

3 Device Fabrication

In this chapter the fabrication of the Ψ-MOSFET devices will be described. Therefore, an overview of the layout will be given first, followed by a description of the main process steps. The fabrication of the devices will be carried out in the clean room facility of the Institute of Semiconductor Electronics. The advisors will instruct the participants how to dress and how to behave in the clean room. In order to avoid contamination participants have to wear gloves at all times working in the clean room. Protective clothing such as apron, a second pair of gloves with sleeves and a face shield is mandatory when working with hazardous chemicals.

Each participant will get one bulk silicon sample for the Ψ-MOSFETs. In addition, one SOI substrate will be fabricated by the supervisor. During your lab-work, protocol the fabrication process and take as many notes as necessary since this will be attached to the written report as an appendix.

3.1 Ψ-MOSFET Layout

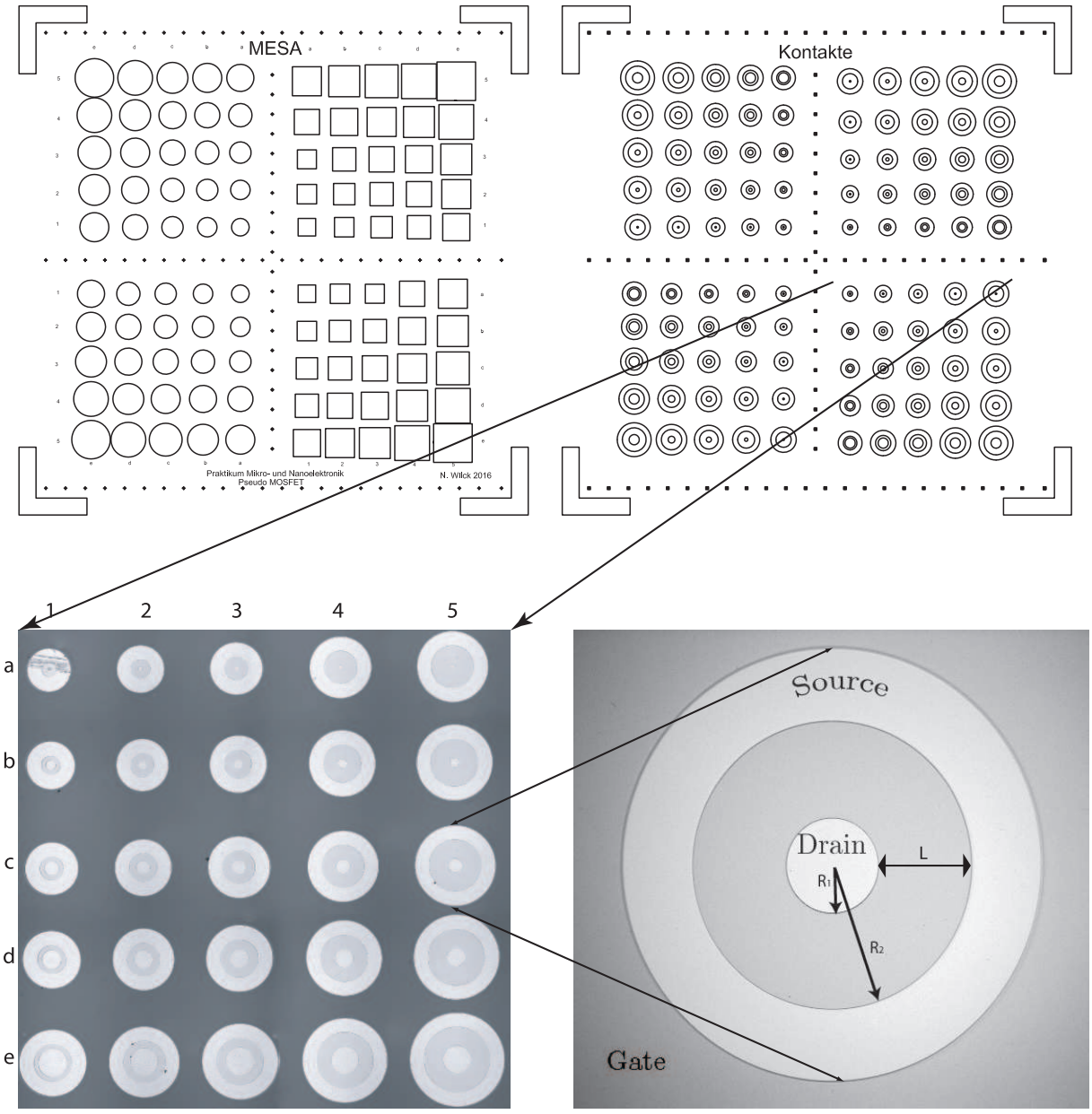
In order to fabricate the devices one bright field mask for optical lithography will be used as shown in Figure 10 in order to structure the mesa areas with reactive ion etching and to define the electrodes for contact metallization.

3.2 Process Steps

The participants will be given prepared bulk silicon and SOI samples with mesas already structured and 100 nm aluminum on top. The thickness of the top-Si (SOI) is about 85 nm and the BOX thickness is 145 nm, respectively.

3.2.1 Pre-processing

The formation of the mesas was done by reactive ion etching (RIE) using a gas mixture of SF_6/O_2. Therefore, in a previous step an etching mask was lithographically defined. Afterwards the remaining resist on the samples was removed by oxygen plasma using a plasma asher. When using the above process to dry etch silicon, the resist will become exposed to a plasma ambient at higher temperature, which causes the resist to harden. This in turn complicates the subsequent resist removal, because solvents (acetone, isopropyl alcohol) might not be able to remove the resist completely if it gets hardened. In order to remove resist thoroughly after dry-etching, an oxygen plasma is used. O_2 plasma exhibits a very good resist removal capability, since the oxygen radicals directly interact with organic solids to form mostly gaseous reaction products which will be pumped away. The oxygen plasma process is therefore also known as plasma ashing.



	1				2				3				4				5			
	R1	R2	lenght	width	R1	R2	lenght	width	R1	R2	lenght	width	R1	R2	lenght	width	R1	R2	lenght	width
a	25	75	50	285,96	25	100	75	339,93	25	125	100	390,40	25	175	150	484,34	25	225	200	571,92
b	50	100	50	453,24	50	125	75	514,29	50	150	100	571,92	50	200	150	679,86	50	250	200	780,79
c	75	125	50	615,00	75	150	75	679,86	75	175	100	741,56	75	225	150	857,88	75	275	200	967,18
d	100	150	50	774,81	100	175	75	842,08	100	200	100	906,47	100	250	150	1028,58	100	300	200	1143,84
e	150	200	50	1092,04	150	225	75	1162,22	150	250	100	1230,01	150	300	150	1359,71	150	350	200	1483,11

Figure 10: Ψ-MOSFET layout and dimensions. All size indications are in μm.

Prior to the deposition of aluminum the samples have to be RCA-cleaned ending with a dip in hydrofluoric acid (HF) in order to leave a bare silicon surface with hydrophobic characteristics. This is done in order to remove any contaminations remaining on the silicon surface and also to remove the oxide which has been grown during the RCA-cleaning caused by the etching solutions based on hydrogen peroxide. Thereby a good electrical contact between aluminum and silicon can be achieved.

> Working with hydrofluoric acid (HF) requires extreme attention! This acid is one of the most dangerous acids to be used in direct handling. A palm-sized area of your body exposed to HF can lead to a lethal injury. Working in a fume hood is mandatory, as well as the use of adequate personal safety equipment when handling this agent. In this case: apron, face shield and acid gloves.

Immediately after this so-called HF-dip the samples have to be put into the evaporation chamber which then needs to be evacuated to prevent a re-oxidization of the sample surface. Once the vacuum has reached the desired process pressure (usually in the range of 10^{-6}...10^{-7} mbar to ensure a large mean free path) the deposition of aluminium can be carried out. The target thickness is 100 nm.

The participants' work is now to define a second resist-mask using optical lithography, which serves as the etching mask for wet-chemical etching of aluminum (the definition of source/drain electrodes). Follow these steps carefully, advice and additional information will be given throughout the entire course.

3.2.2 2nd Lithography

- bake samples on a hot plate for 5 mins @ 130 °C to desorb any water on the surface;
- apply adhesion promoter hexamethyldisilazane (HMDS);
- let samples cool for a minute;
- apply 7-8 drops of photoresist (AZ 5214E™), spin @ 3000 rpm for 30 s;
- soft-bake resist, 90 s @ 95 °C;
- expose samples using the correct mask (contact layer), with following parameters: 6 s (exposure time) @ 15 $\frac{\text{mW}}{\text{cm}^2}$ (power density), 405 nm (wavelength, h-line), hard-contact mode;
- develop samples, 50 s in developer AZ 726MIF™ (MIF stands for: metal ion free).

3.2.3 Aluminum Etch

The etchant (acids) used in this section is a mixture of concentrated acids which will heat up during mixing. Additionally, the hot solutions are likely to evaporate. Working in a fume hood with appropriate personal safety equipment (multiple gloves, apron and goggles/shield) is mandatory!

- Prepare aluminum etchant solution (phosphoric acid, nitric acid, acetic acid and water in a volume ratio of 16:1:1:2);
- Prepare a beaker with deionized water (300...400 ml);
- Put samples into holder and the holder into the etchant;
- Wait until the aluminum has been removed and only the circles and dots from the mask are remaining. You might want to check beforehand what pattern you can expect to see by looking at the mask (Figure 10);
- Put the sample holder together with the samples into the deionized water and let rinse for 10 min under the DI-water tap;
- Take out the samples and blow them dry with nitrogen.

3.2.4 Resist Removal

Working with hot solvents requires the same precaution as if you were working with acids. Heated up solvents might be in a state of overheating in which they can spontaneously evaporate and splash. Always heat up solvents with a sample holder or at least with an object inserted into the liquid (tweezers, etc.).

- Put the samples into hot acetone, boil for 10 mins;
- Put the samples into isopropylic alcohol, boil for 10 mins;
- Take samples out and blow them dry with nitrogen;
- If resist is remaining (check with optical microscope), ash the residual resist in O_2 plasma for at least one hour.

In Figure 11 a schematical overview of the whole process flow is given.

4 Electrical Measurement and Characterization

Electrical measurements will be carried out with the Keithley™ 4200-SCS Semiconductor Characterization System. The sample will be mounted in a probe station as schematically shown in Figure 12. The following measurements and characterizations should be carried out:

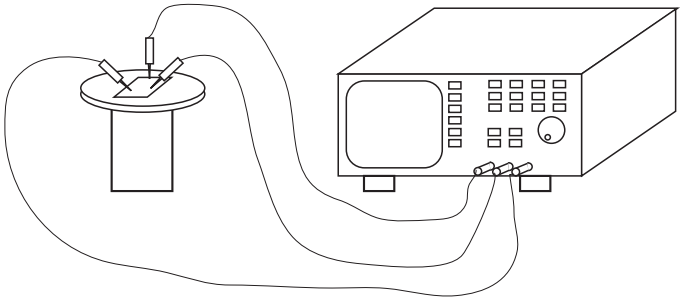
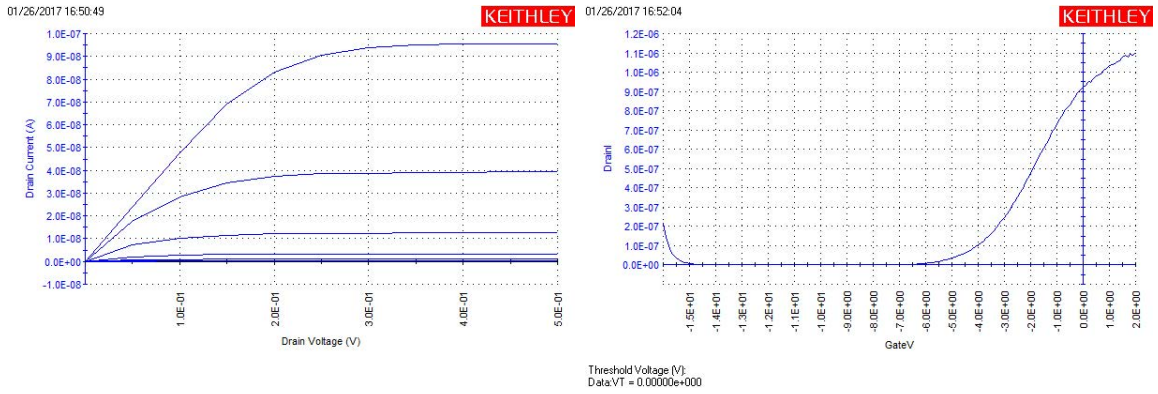


Figure 12: Schematic of the measurement set-up.

1. Contact measurement probes to source/drain/gate pads. It is possible to improve the back-gate contact by using conductive silver paste;

2. Measure and plot the transfer characteristics $I_d - V_{gs}$, tell a rough value of the threshold voltage;

3. Measure and plot the output characteristics $I_d - V_{ds}$, start the voltage step for V_{gs} with a value smaller than the estimated threshold voltage, tell if the drain-source voltage applied in step 2 falls into the linear region of the output characteristics $I_d - V_{ds}$, otherwise replot the transfer characteristics $I_d - V_{gs}$ with a new V_{ds};



(a) output characteristic at V_{gs}=-7, ..., -2 V (b) transfer characteristic at V_{ds}=0.5 V

Figure 13: Output and transfer characteristics

4. Extract the mobility of the fabricated samples using the $I_d/\sqrt{g_m}$ - method. Plot mobility value against channel length for different devices on the sample.

5 Self Test

1. What is the Ψ-MOSFET used for in the scope of this lab course?
2. Why do we need O_2 mixed with SF_6 to etch silicon?
3. How can native oxide be removed?
4. Which scale of the y-Axis has to be used in order to determine the transconductance g_m, linear or log? How about subthreshold slope?
5. How does the mobility depend on I_{ds} and g_m?
6. Which parameters of your substrate influence the device characteristic?
7. What parameters should be measured after device fabrication?
8. How do you measure these parameters?
9. What is the main goal of this experiment?
10. Are there any other methods to define the source/drain contacts?

6 Report Writing

The report should include both the fabrication and the characterization part of this lab course. In the first part of the lab course we deal with the technology used to fabricate these devices, which means in turn lithography, reactive ion etching, RCA-cleaning, metallization of the samples and wet-chemistry used for etching of the aluminum, respectively. The second part of this course is foreseen to electrically characterize the samples. Therefore we will first discuss some theoretical aspects of device physics and operation principles followed by measuring the characteristics of the devices. Finally, you have to determine the mobility of the charge carriers using the $I_\mathrm{d}/\sqrt{g_\mathrm{m}}$ - method.

Annex

Bibliography

- M.S. Sze, "Physics of Semiconductor Devices", John Wiley & Sons Inc., 1981.
- Y. Taur and T.H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 1998.
- J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI", Kluwer Academic Publisher, 2004.
- W. Kern, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology ", RCA Review, Vol. 31, p187, 1970.
- D. K. Schroder, "Semiconductor Material Device Characterization", Wiley IEEE-Press, 2006.
- D.A. Neamen, "Semiconductor Physics and Devices", Mc Graw Hill, 2012
- J.Knoch and S. Mantl and S. Feste, "Metal-Oxide-Semiconductor Field-Effect Transistors: Novel Materials and Alternative Concepts", Wiley-VCH, 2012.

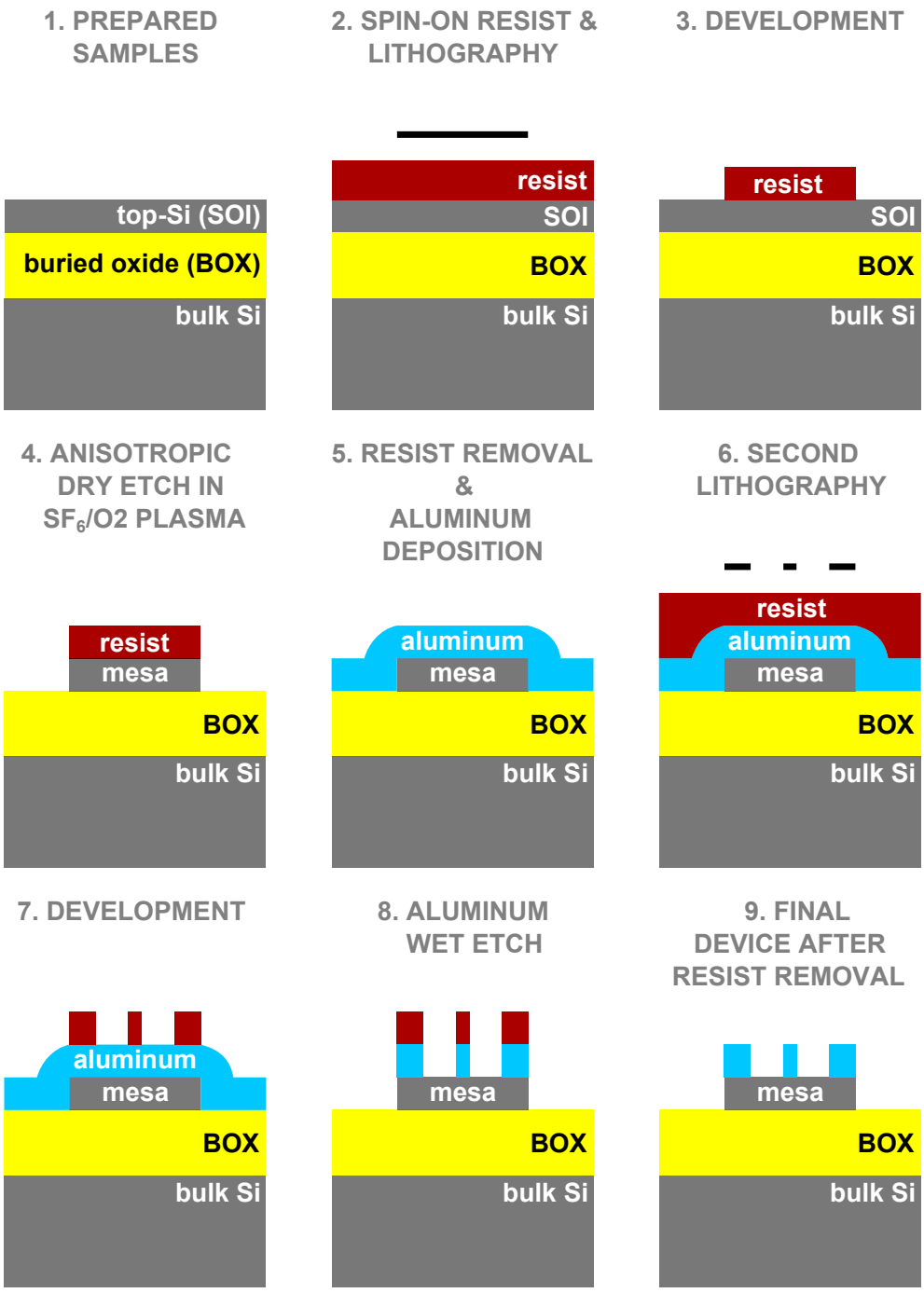


Figure 11: Schematics of device fabrication process flow.